Amendments to the claims (this listing replaces all prior versions):

1. (Currently Amended) A programmable intra-packet switching method comprising:

determining which, if any, of a plurality of data ports connected to a network~~,~~ contains a data packet available for processing;

fragmenting a first portion of a first available data packet into at least one data cell having a defined size; wherein this fragmentation of the first data packet continues until a user-defined number of cells are generated;

storing at least one data element concerning the first available data packet, wherein the data element enables subsequent fragmenting of a second portion of the first available data packet; and

subsequent to fragmenting the first portion of the first data packet and prior to fragmenting [[a]] the second portion of the first available data packet, fragmenting at least a portion of a second available data packet on a different one of the plurality of data ports.

2. (Original) The programmable intra-packet switching method of claim 1 further comprising:

monitoring the number of data cells produced to determine if the user defined number of cells have been generated.

3. (Previously Presented) The programmable intra-packet switching method of claim 2 wherein monitoring the number of data cells produced includes:

re-determining which, if any, of the plurality of data ports contains a data packet available for processing, if it is determined that the user defined number of cells have been generated, to determine if any other port contains a data packet available for processing.

4. (Original) The programmable intra-packet switching method of claim 3 wherein monitoring the number of data cells produced includes:

storing at least one data element concerning the data packet currently being processed if it is determined that another port contains a data packet available for processing, wherein this data element allows for subsequent processing of the remainder of the data packet currently being processed.

5. (Original) The programmable intra-packet switching method of claim 4 wherein monitoring the number of data cells produced includes:

initiating the fragmentation process, if it is determined that another port contains a data packet for processing, to fragment the data packet on the other port into at least one data cell having a defined size; wherein the packet fragmentation process continues fragmenting the data packet on the other port into data cells until the user-defined number of cells are generated.

6. (Original) The programmable intra-packet switching method of claim 1 further comprising:

determining if the data packet has been fully fragmented into at least one data cell.

7. (Previously Presented) The programmable intra-packet switching method of claim 6 wherein determining if the data packet has been fully fragmented includes:

re-determining which, if any, of the plurality of data ports contains a data packet available for processing, if it is determined that the data packet has been fully fragmented into at least one data cell, to determine if any other port contains a data packet available for processing.

8. (Original) The programmable intra-packet switching method of claim 7 wherein determining if the data packet has been fully fragmented includes:

initiating the fragmentation process, if it is determined that another port contains a data packet for processing, to fragment the data packet on the other port into at least one data cell having a defined size; wherein the packet fragmentation process continues fragmenting the data packet on the other port into data cells until the user-defined number of cells are generated.

9. (Currently Amended) A programmable intra-packet switching process comprising:

a port polling process for determining which, if any, of a plurality of data ports connected to a network contains a data packet available for processing;

a packet fragmentation process, responsive to said port polling process determining that a first one of said ports contains a first data packet, for fragmenting said first data packet into at least one data cell having a defined size; wherein said packet fragmentation process continues fragmenting said first data packet into said data cells until a user-defined number of cells are generated; [[and]]

a packet information storage process for storing at least one data element concerning the first data packet, wherein said data element enables subsequent fragmenting of a second portion of the first data packet; and

a second packet fragmentation process for fragmenting at least a portion of a second available data packet on a different one of the plurality of data ports subsequent to fragmenting the first portion of the first data packet and prior to fragmenting [[a]] the second portion of the first available data packet.

10. (Original) The programmable intra-packet switching process of claim 9 further comprising:

a cell limit monitoring process for monitoring the number of data cells produced by said packet fragmentation process to determine if said user defined number of cells have been generated.

11. (Original) The programmable intra-packet switching process of claim 10 wherein said cell limit monitoring process includes:

a cell limit port switching process, responsive to said cell limit monitoring process determining that said user defined number of cells have been generated, for initiating said polling process to determine if any other port contains a data packet available for processing.

12. (Canceled)

13. (Currently Amended) The programmable intra-packet switching process of claim [[12]] 9 wherein said at least one data element includes:

a data packet remainder length indicator, indicative of the length of the portion of said data packet not fragmented; and

a packet truncation indicator, indicative of the incomplete fragmentation status of said data packet.

14. (Original) The programmable intra-packet switching process of claim 11 wherein said cell limit monitoring process includes:

a cell limit fragmentation switching process, responsive to said cell limit port switching process determining that another port contains a data packet for processing, for initiating said packet fragmentation process to fragment said data packet on said other port into at least one data cell having a defined size; wherein said packet fragmentation process continues fragmenting said data packet on said other port into said data cells until said user-defined number of cells are generated.

15. (Original) The programmable intra-packet switching process of claim 9 further comprising:

a packet completion monitoring process for monitoring the status of said packet fragmentation process to determine if said data packet has been fully fragmented into said at least one data cell.

16. (Original) The programmable intra-packet switching process of claim 15 wherein said packet completion monitoring process includes:

a packet completion port switching process, responsive to said packet completion monitoring process determining that said data packet has been fully fragmented into said at least one data cell, for initiating said polling process to determine if any other port contains a data packet available for processing.

17. (Original) The programmable intra-packet switching process of claim 16 wherein said packet completion monitoring process includes:

a packet completion fragmentation switching process, responsive to said packet completion port switching process determining that another port contains a data packet for processing, for initiating said packet fragmentation process to fragment said data packet on said other port into at least one data cell having a defined size; wherein said packet fragmentation process continues fragmenting said data packet on said other port into said data cells until said user-defined number of cells are generated.

18. (Original) The programmable intra-packet switching process of claim 9 further comprising:

a user interface for allowing a user to specify at least one user-defined parameter utilized by said packet fragmentation process.

19. (Original) The programmable intra-packet switching process of claim 18 wherein said at least one user-defined parameter includes:

said user-defined number of cells to be generated by said packet fragmentation process; and

said defined size of said at least one data cell.

20. (Original) The programmable intra-packet switching process of claim 9 wherein said at least one data cell having a defined size is a 53-byte Asynchronous Transfer Mode (ATM) cell.

21. (Currently Amended) A programmable packet fragmentation process comprising:

a process for determining the availability of a data packet on a plurality of data ports connected to a synchronous optical network;

a packet fragmentation process, responsive to said process, said packet fragmentation process including:

determining the availability of said data packet on one of said plurality of ports, for fragmenting a first portion of a first data packet into at least one Asynchronous Transfer Mode (ATM) cell, wherein said packet fragmentation process continues fragmenting said data packet into said data cells until a user-defined number of cells are generated; [[and]]

a packet information storage process for storing at least one data element concerning the first data packet, wherein said data element enables subsequent fragmenting of a second portion of the first data packet; and

subsequent to fragmenting the first portion of the first data packet and prior to fragmenting [[a]] the second portion of the first available data packet, fragmenting at least a portion of a second available data packet on a different one of the plurality of data ports.

22. (Original) The programmable intra-packet switching process of claim 21 further comprising:

a cell limit monitoring process for monitoring the number of data cells produced by said packet fragmentation process to determine if said user defined number of cells have been generated.

23. (Original) The programmable intra-packet switching process of claim 21 further comprising:

a packet completion monitoring process for monitoring the status of said packet fragmentation process to determine if said data packet has been fully fragmented into said at least one data cell.

24. (Currently Amended) A programmable intra-packet switching process comprising:

a port polling process for determining which port, if any, of a plurality of data ports connected to a network contains a data packet available for processing;

a packet fragmentation process, responsive to said port polling process:

for determining that one of said ports contains a data packet,

for fragmenting a first portion of a first data packet into at least one data cell; wherein said packet fragmentation process continues fragmenting said first data packet into said data cells until a port-switching event occurs; [[and]]

a packet information storage process for storing at least one data element concerning the first data packet, wherein said data element enables subsequent fragmenting of a second portion of the first data packet; and

subsequent to a port-switching event packet and prior to fragmenting [[a]] the second portion of the first available data packet, for fragmenting at least a portion of a second available data packet on a different one of the plurality of data ports.

25. (Original) The programmable intra-packet switching process of claim 24 wherein said port-switching event is an unbalanced port-loading condition.

26. (Original) The programmable intra-packet switching process of claim 24 wherein said port-switching event is the generation of a user-defined number of cells.

27. (Original) The programmable intra-packet switching process of claim 26 further comprising:

a cell limit monitoring process for monitoring the number of data cells produced by said packet fragmentation process to determine if said user defined number of cells have been generated.

28. (Original) The programmable intra-packet switching process of claim 24 further comprising:

a packet completion monitoring process for monitoring the status of said packet fragmentation process to determine if said data packet has been fully fragmented into said at least one data cell.

29. (Currently Amended) A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

determine which port, if any, of a plurality of data ports connected to a network contains a data packet available for processing;

fragment a first portion of a first available data packet into at least one data cell having a defined size; wherein this fragmentation continues until a user-defined number of cells are generated;

storing at least one data element concerning the first available data packet, wherein the data element enables subsequent fragmenting of a second portion of the first available data packet; and

fragment at least a portion of a second available data packet on a different one of the plurality of data ports, wherein this fragmentation occurs subsequent to the fragmentation of the first portion of the first data packet and prior to the fragmentation of [[a]] the second portion of the first available data packet.

30. (Original) The computer program product of claim 29 wherein said computer readable medium is a read-only memory.

31. (Original) The computer program product of claim 29 wherein said computer readable medium is a random access memory.

32. (Currently Amended) A processor and memory configured to:

determine which port, if any, of a plurality of data ports connected to a network contains a data packet available for processing;

fragment a first portion of a first available data packet into at least one data cell having a defined size; wherein this fragmentation continues until a user-defined number of cells are generated;

storing at least one data element concerning the first available data packet, wherein the data element enables subsequent fragmenting of a second portion of the first available data packet; and

fragment at least a portion of a second available data packet on a different one of the plurality of data ports, wherein this fragmentation occurs subsequent to the fragmentation of the first portion of the first data packet and prior to the fragmentation of [[a]] the second portion of the first available data packet.

33. (Original) The processor and memory of claim 32 wherein said processor and memory are incorporated into a single board computer.

34. (Original) The processor and memory of claim 32 wherein said processor and memory are incorporated into an Asynchronous Transfer Mode / Packet Over Sonet (ATM/POS) processor.